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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,300	12/31/2003	KyeHyung Lee	INTEL-0059	8431

34610 7590 02/16/2005

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,300	LEE ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-13,15-26 and 28-30* is/are rejected.

7)☒ Claim(s) *5,14 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1- 30 are presented in the instant application according to the Applicants' filing on 12/31/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Abstract

2. The amended abstract of the disclosure is objected to because of the following:

3. Line 2, it is suggested changing "adapted" to –configured-- in order to reflect positive disclosure of the claimed invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huffman (U.S. Patent No. 6,480,433) in view of Hellums (U.S. Patent No. 5,362,988).

With respect to claims 1 and its corresponding method claim 10, Huffman discloses, in Fig. 4, a circuit comprising a) a first filter [305] to filter first component [313] of two differential input signals [input signals at 313 and 314]; b) a second filter [306] to filter second component of the differential input signals [input signals at 313 and 314]; and a delay cell [310] to generate a delayed differential signal based on outputs of the first and second filters.

Huffman fails to teach first components *(in plural form)* and second components *(in plural form),* the components are transistors.

Hellums discloses, in Fig. 1, a transistor unit having a plurality of transistors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a transistor unit of Huffman having a plurality of transistors for higher dynamic range as taught by Hellums since such circuit arrangement has been a well-known practice as evidenced by the teachings of Hellums.

With respect to claims 2 and 11, the combined teaching of Huffman and Hellums discloses that the first and second filters smooth a state transition in the delayed differential signal, the state transition corresponding to an offset that exists between the differential input signals.

With respect to claims 3 and 12, the combined teaching of Huffman and Hellums discloses that the offset is one of a time offset and phase offset.

With respect to claims 4 and 13, the combined teaching of Huffman and Hellums discloses that the delayed differential signal is a continuous time-varying signal.

6. Claims 1, 6-10, 15-21, 23-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna (U.S. Patent No. 5,051,628) in view of Hellums (U.S. Patent No. 5,362,988).

With respect to claims 1 and its corresponding method claim 10, Hanna discloses, in Fig. 2, a circuit comprising a) a first filter [22] to filter first component [62] of two differential input signals [input signals at 62 and 64]; b) a second filter [20] to filter second component of the differential input signals [input signals at 62 and 64]; and a delay cell [62, 64, 66, 68, 80, 70] to generate a delayed differential signal based on outputs of the first and second filters.

Hanna fails to teach first components *(in plural form)* and second components *(in plural form)*, the components are transistors.

Hellums discloses, in Fig. 1, a transistor unit having a plurality of transistors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a transistor unit of Hanna having a plurality of transistors for higher dynamic range as taught by Hellums since such circuit arrangement has been a well-known practice as evidenced by the teachings of Hellums.

With respect to claims 6, 15 and 16, the combined teaching of Hanna and Hellums discloses that the first filter [22] includes a resistor [22] having a resistance value which smooths a state transition in a second component of the delayed differential signal.

With respect to claims 7, 17 and 18, the combined teaching of Hanna and Hellumms discloses that the second filter [20] includes a resistor [20] having a resistance value which smooths a state transition in a second component of the delayed differential signal.

With respect to claims 8 and 19, the combined teaching of Hanna and Hellums discloses that the delay cells includes a) a load [68,80,70]; b) a current source [66]; c) a first switching circuit [62] to connect the current source [66] to the load based on the first filtered components of the differential input signals; d) a second switching circuit [64] to connect the current source [66] to the load based on the second filtered components of the differential input signals; and terminals [top (=), top (-)] to output the delayed differential signal generated based on current flowing between the current source and load.

With respect to claims 9 and 20, the combined teaching of Hanna and Hellums discloses that the load includes a symmetric configuration of transistors.

With respect to claim 21, Hanna discloses, in Figs. 1 and 2, a circuit comprising a) a first delay cell which includes a first filter [22] to filter first component [62] of first and second differential signals [signals at 62 and 64]; b) a second filter [20] to filter second component of the first and second differential signals [signals at 62 and 64]; and a delay cell [62, 64, 66, 68, 80, 70] to generate a delayed differential signal based on outputs of the first and second filters; and a second delay cell [in Fig. 1] which generates a differential signal which includes the first and second components of the first differential signal input into the first delay cell

Hanna fails to teach first components *(in plural form)* and second components *(in plural form)*, the components are transistors.

Hellums discloses, in Fig. 1, a transistor unit having a plurality of transistors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a transistor unit of Hanna having a plurality of transistors for higher dynamic range

as taught by Hellums since such circuit arrangement has been a well-known practice as evidenced by the teachings of Hellums.

With respect to claim 23, the combined teaching of Huffman, Hellums and Nair et al. discloses that the first and second filters smooth a state transition in the delayed differential signal, the state transition corresponding to an offset that exists between the first and second differential signals.

With respect to claim 24, the combined teaching of Huffman, Hellums and Nair et al. discloses that the offset is one of a time offset and phase offset.

With respect to claim 25, the combined teaching of Hanna and Hellums discloses that the first filter [22] includes a resistor [22] having a resistance value which smooths a state transition in a second component of the delayed differential signal.

With respect to claim 26, the combined teaching of Hanna and Hellums discloses that the second filter [20] includes a resistor [20] having a resistance value which smooths a state transition in a second component of the delayed differential signal.

With respect to claim 28, Hanna discloses, in Figs. 1 and 2, a system comprising a) a first circuit [Fig. 1, right side of items 56,52], and b) a second circuit including a first filter [22] to filter first component of two differential input signals [signals at 62 and 64]; a second filter [20] to filter second components of the differential input signals [signals at 62 and 64]; and a delay cell [62, 64, 66, 68, 80, 70] to generate a delayed differential signal based on outputs of the first and second filters, the delayed differential signal controlling the first circuit.

Hanna fails to teach first components *(in plural form)* and second components *(in plural form)*, the components are transistors.

Hellums discloses, in Fig. 1, a transistor unit having a plurality of transistors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a transistor unit of Hanna having a plurality of transistors for higher dynamic range as taught by Hellums since such circuit arrangement has been a well-known practice as evidenced by the teachings of Hellums.

With respect to claim 29, the combined teaching discloses that the first circuit includes a chipset.

With respect to claim 30, the combined teaching discloses the first circuit includes a memory controller.

7. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna and Hellums, as applied to claim 21, in view of Nair et al. (of record, IDS filed 12/31/03).

With respect to claim 22, the combined teaching of Hanna and Hellums discloses all of the claimed limitations as expressly recited in claim 21.

However, Hanna and Hellums does not explicitly disclose the delay line include a third delay cell.

Nair et al. discloses, in Fig. 6, a delay line [630] with a plurality of more than three differential delay cells.

To modify the delay line of the combined teaching of Hanna and Hellums to include a third delay cell in the delay line to increase frequencies of operation and reduce uncertainty margins and tighter design tolerances, as taught by Nair et al. would have been obvious to one of

ordinary skill in the art at the time of the invention since such arrangement of the delay line for the stated purpose has been a well known practice as evidenced by the teachings Nair et al.

Allowable Subject Matter

8. Claims 5, 14 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

A circuit, in which the first components are positive components of the differential input signals and the second components are negative components of the differential input signals, as called for in claims 5, 14 and 27.

Citation of Relevant Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Hirabayashi (U.S. Patent No. 6,724,230) discloses a semiconductor integrated circuit with delay elements.

Prior art Norigi et al. (U.S. Patent No. 6,611,468) discloses a non-volatile semiconductor memory device having sensitive sense amplifier structure.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER